

FEATURES

Fixed gain of 29 dB

Operation from 2.5 GHz to 2.7 GHz

EVM $\leq 3\%$ with 16 QAM OFDMA

@ $P_{OUT} = 25 \text{ dBm}$ [3.5V] and

@ $P_{OUT} = 27.5 \text{ dBm}$ [5V]

Input internally matched to 50 Ω

Power supply: 3.2 V to 5 V

Quiescent current

130 mA in normal power mode

PAE: $> 20\%$

Multiple operating modes to reduce battery drain

Standby mode: 10 mA

Sleep mode: $< 1 \mu\text{A}$

APPLICATIONS

WiMAX/WiBro Mobile Terminals and CPEs

GENERAL DESCRIPTION

The ADL5571 is a high linearity 2.5 GHz to 2.7 GHz power amplifier designed for WiMAX terminals and CPEs using TDD operation at a duty cycle of 50% or lower. With a gain of 29 dB and an output compression point of 31 dBm, it can operate at an output power level up to 26 dBm while maintaining an EVM of $\leq 3\%$ with a supply voltage of 5V. PAE is greater than 20% at $P_{OUT} = 25 \text{ dBm}$ with a 3.5V supply voltage.

The ADL5571 RF input is matched on chip and provides an input return loss of less than -10 dB . The open-collector output is externally matched with strip-line and external shunt capacitance.

FUNCTIONAL BLOCK DIAGRAM

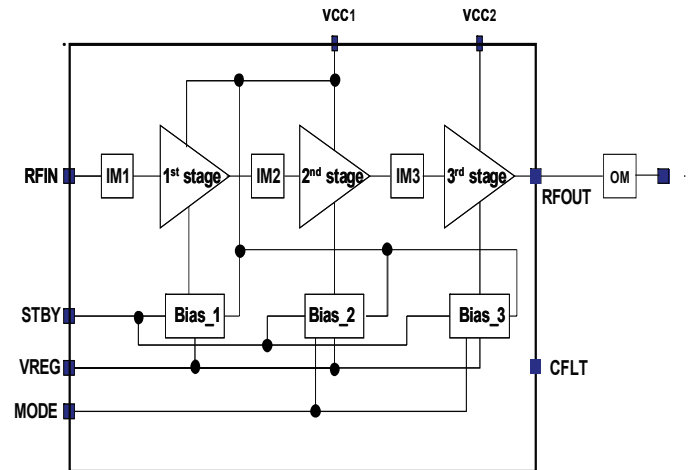


Figure 1. ADL5571 Block Diagram

The ADL5571 operates over a supply voltage range from 3.2 V to 5 V with a current of 440mA Burst RMS when delivering 25 dBm (3.5 V supply). A Standby mode is available which reduces the quiescent current to 10 mA: useful when a TDD terminal is receiving data.

The ADL5571 is fabricated in a GaAs HBT process and is packaged in a 4mm x 4mm 16-Lead Pb-free RoHS compliant LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from -40°C to $+85^\circ\text{C}$.

Rev. PrB

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	5
Applications.....	1	ESD Caution.....	5
Functional Block Diagram	1	Pin Configuration and Function Descriptions.....	6
General Description	1	Typical Performance Characteristics	7
Revision History	2	Evaluation Board	8
Target Specifications—VCC = 3.5 V	3	Outline Dimensions	10
Target Specifications - Vcc = 5 V	4		

REVISION HISTORY

09/07—Rev. PrB: Preliminary Version

06/07—Rev. PrA: Preliminary Version

TARGET SPECIFICATIONS—VCC = 3.5 V

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, $Z_L = 50 \Omega$, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	See table 5 for tuning details	2.5		2.7	GHz
Linear Output Power	EVM \leq 3%		25		dBm
Gain			29.5		dB
vs. Frequency	± 5 MHz		± 0.3		dB
vs. Temp	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.5		dB
vs. Supply	3.2 V to 4.2 V		± 1		dB
OP1dB	Unmodulated input		31		dBm
EVM	$P_{OUT} = 25$ dBm		3		% rms
Input Return Loss			10		dB
ACPR	Center Frequency=2.6Ghz, Output power =24dBm				
	± 5.05 MHz carrier offset		-33		dBm
	± 6.5 MHz carrier offset		-23.5		dBm
	± 11 MHz carrier offset		-27		dBm
	± 20.5 MHz carrier offset		-38		dBm
Harmonic Distortion			36		dBc
Power Supply Interface	VCC = 3.5 V				
Supply Current	$P_{OUT} = 25$ dBm,		420		mA
PAE	$P_{OUT} = 25$ dBm		20		%
Standby Mode	VREG = 2.85 V		10		mA
Sleep Mode	VREG = 0 V		10		μA
Turn On/Off Time			1		μs
VSWR Survivability		10:1			

TARGET SPECIFICATIONS - VCC = 5 V

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, $Z_L = 50 \Omega$, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	See table 5 for tuning details	2.5		2.7	GHz
Linear Output Power	EVM \leq 3%		27.5		dBm
Gain			29		dB
vs. Frequency	± 5 MHz		± 0.3		dB
vs. Temp	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.5		dB
vs. Supply	4.5 V to 5.5 V		± 1		dB
OP1dB	Unmodulated input		32		dBm
EVM	$P_{OUT} = 27.5$ dBm		3		% rms
Input Return Loss			10		dB
ACPR	Center Frequency=2.6GHz, Output power = 24 dBm		38		dBc
	± 5.05 MHz carrier offset		-25		dBm
	± 6.5 MHz carrier offset		-17		dBm
	± 11 MHz carrier offset		-27		dBm
	± 20.5 MHz carrier offset		-38.5		dBm
Harmonic Distortion					
Power Supply Interface	VCC = 5 V				
Supply Current	$P_{OUT} = 27.5$ dBm		420		mA
PAE	$P_{OUT} = 27.5$ dBm		20		%
Standby Mode	VREG = 2.85 V, STBY = 2.5 V		10		mA
Sleep Mode	VREG = 0 V		10		μA
Turn On/Off Time			1		μs
VSWR Survivability		10:1			

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
V _{CC}	5.0 V
V _{REG}	3 V
STBY	3 V
RFOUT (Modulated—Normal Power Mode) ¹	29 dBm
Output Load VSWR	10:1
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Solder Reflow Temperature	260°C (30 sec)

¹ OFDMA carrier, 16 QAM, 10 MHz channel BW, 1024 FFT.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

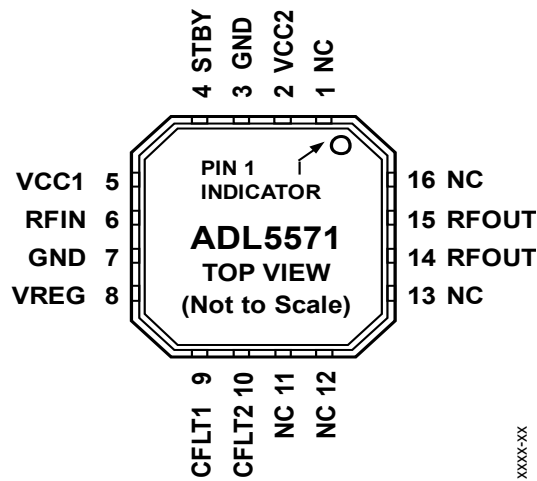


Figure 2. ADL5571 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
5	VCC1	Connect to Power Supply.
6	RFIN	Matched RF Input.
8	VREG	When VREG is low, the device goes into sleep mode, reducing supply current to 1 uA. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA.
9,10	CFLT1, CFLT2	A Ground Referenced Capacitor. It should be connected to this node to reduce bias line noise .
14, 15	RFOUT	Unmatched RF Output. These parallel outputs can be matched to 50 Ω using strip-line and shunt capacitance. The power supply voltage should be connected to these pins through a choke inductor.
2	VCC2	This power supply pin should be connected to the supply via a choke circuit (see Figure 8).
4	STBY	When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing supply current to 10 mA.
1, 11, 13, 16	N/C	No Connect. Do not connect these pins.
7	GND	Connected to Ground.
	Exposed Paddle	The exposed paddle should be soldered down to a low impedance ground plane (use multiple vias (at least 9) to stitch together the ground planes) for optimum electrical and thermal performance.

Table 5. Operating Modes¹

Mnemonic	Normal Operation	Standby Mode	Sleep Mode
VREG	High	High	Low
STBY	Low	High	X

¹ X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, Z_L = 50 Ω, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

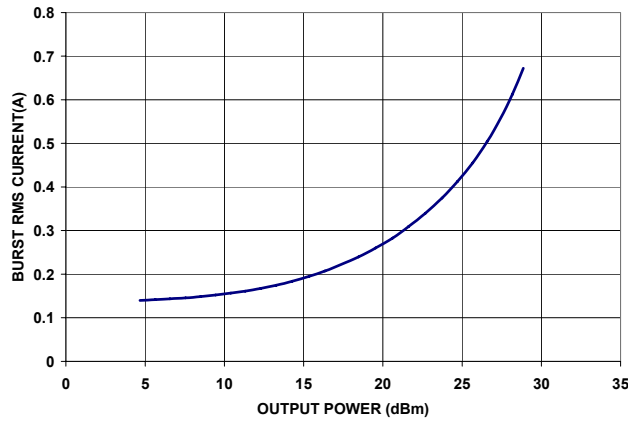


Figure 3. Burst RMS Current vs. P_{OUT} at 2.6GHz, V_{CC}=3.5V

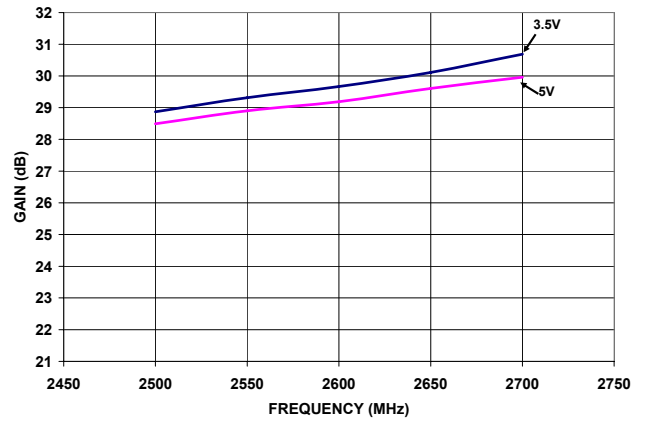


Figure 6. Gain vs. Frequency at P_{IN} = -4 dBm

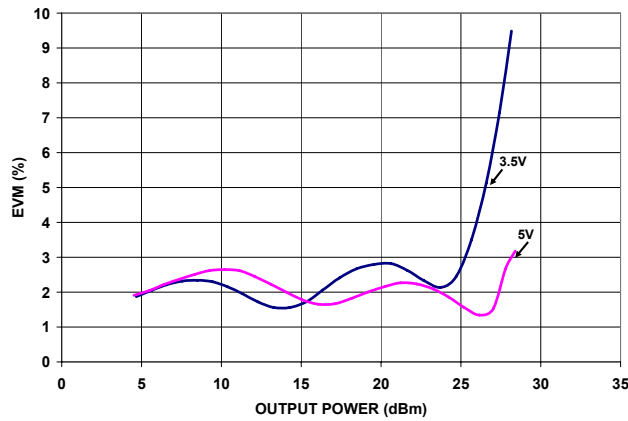


Figure 4. EVM vs. P_{OUT} at 2.6 GHz.

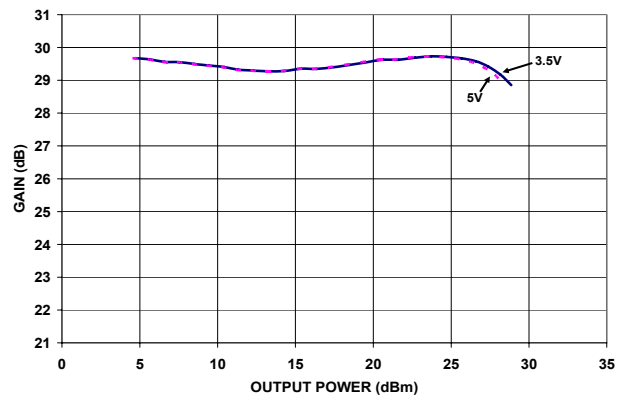


Figure 7. Gain vs Output Power at 2.6 GHz

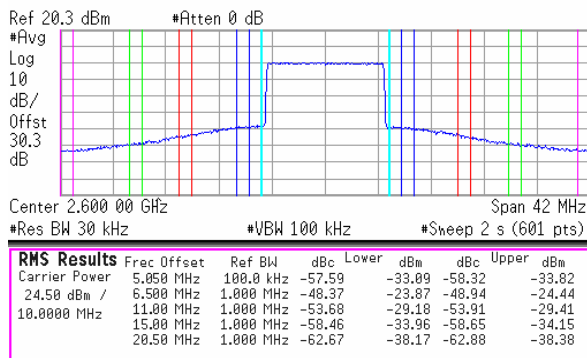


Figure 5. ACPR Measurement at 2.6 GHz, V_{CC} = 5 V with FCC Limits Applied.

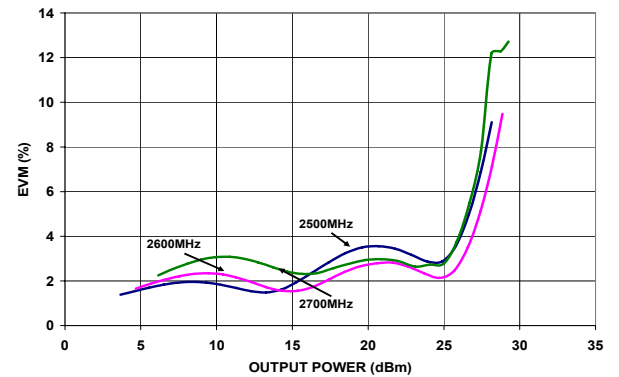


Figure 8. EVM vs. Output Power at V_{CC}=3.5V

EVALUATION BOARD

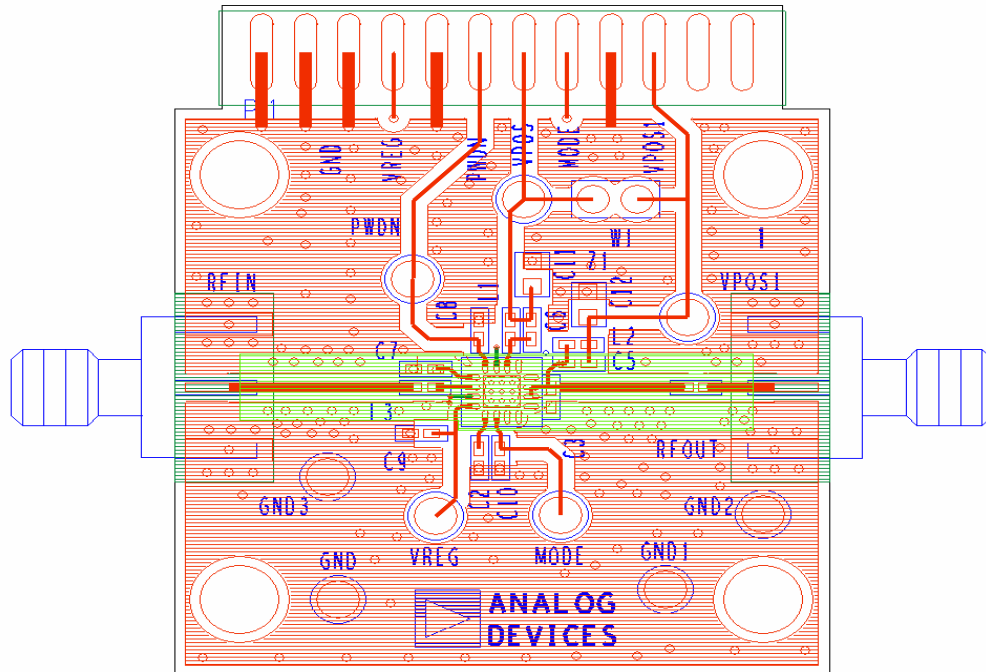


Figure 9. Evaluation Board Layout

The ADL5571 performance data were taken on a FR4 board layout. Care should be taken to ensure 50Ω impedance for all RF traces. For optimal performance in linearity, gain and efficiency, the output matching capacitor, C3, should be placed 35 mils from the edge of the package.

Table 6. Evaluation Board Configuration Options

Component	Function	Default Value
Vpos, Vpos1, GND	Supply and Ground Connections	W1 = Installed
TP1 (STBY)	Transmit/Standby Mode: When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing supply current to 10 mA.	Not Applicable
TP2 (VREG)	Normal/Sleep Mode: When VREG is low, the device goes into sleep mode, reducing supply current to 10 uA. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA	Not Applicable
TP5(MODE)	Do Not Connect.	Not Applicable
L3,	Input Interface: (L3) matches the input to 50 ohms.	L3 = 2.2nH (Size 0402)
C3, C4,	Output Interface: C4 provides dc blocking. C3 matches the output to 50 ohms.	C4 = 39pF (Size 0402) C3 = 2.7pF (Size 0402) (C3 value for 2.5Ghz to 2.7Ghz operation)
C2, C10	Filter Interface: A ground referenced capacitor should be connected to this node to reduce bias line noise	C2 = 2.2pF (Size 0402) C10 = 0.01 μ F (Size 0402)
C7, C8, C9, C11, C12	Power Supply Decoupling: The capacitors, C7, thru C12, are used for power supply decoupling. They should be placed as close as possible to the DUT.	C7 = 0.01 μ F (Size 0402) C8 = 0.01 μ F (Size 0402) C9 = 0.01 μ F (Size 0402) C10 = 0.01 μ F (Size 0402) C11 = 1 μ F (Size 0402) C12 = 1 μ F (Size 0402)
L1, L2, C6, C5	RF Trap: L1, C6 and L2, C5 form tank circuits and prevent RF from propagating on the dc supply lines	L1 = 1nH (Size 0402) C6 = 3.3pF (Size 0402) L2 = 11nH (Size 0402) C5 = OPEN

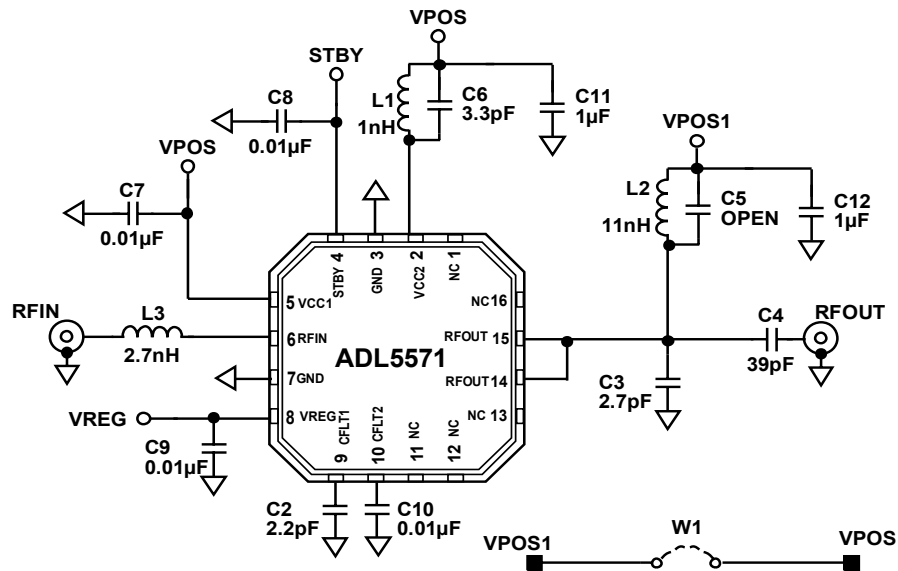


Figure 10. Application Schematic
Rev. PrB | Page 9 of 11

ADL5571 MEASUREMENT SETUP

1. Connect the output of the WiMAX signal generator to the RF input through a cable.
2. Connect the RF output SMA of the ADL5571 to the Spectrum Analyzer (preferably through an attenuator).
3. Ensure that Jumper W1 is in place. Alternatively, use a jumper cable to connect VPOS to VPOS1.
4. Connect power supply to VPOS. Set voltage to the desired supply level (3.5V, 5V). Ensure to keep the current limit on this source to 1A.

Table 7. Operating Modes¹

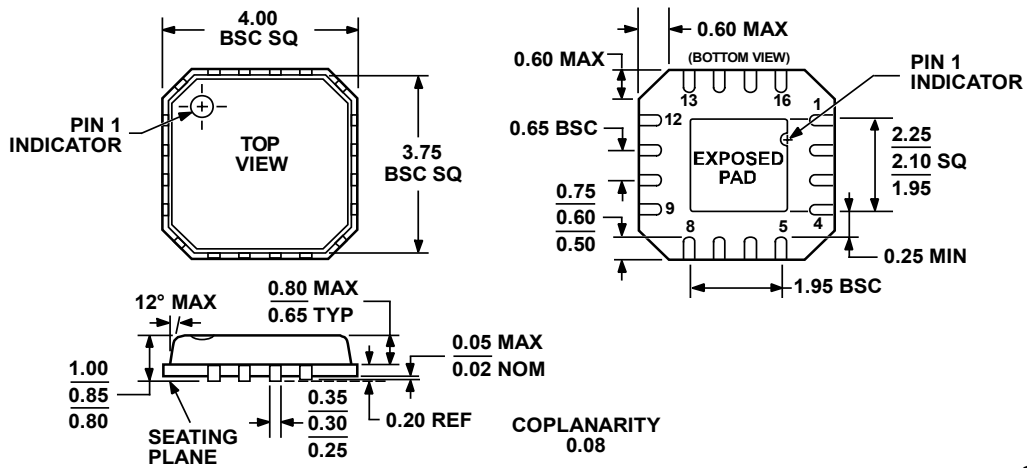
Power Supply

nomenclature	HIGH	LOW	sequence up	sequence down
VREG	2.85 V	0V	-	-
STBY	2.5 V	0V	-	-

Note : Device is not sequence dependent

5. Turn all voltage supplies on.
6. Turn RF Source On.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 4 mm x 4 mm Body, Very Thin Quad
 (CP-16-4)
 Dimensions shown in millimeters

021207-A